WHAT IS CLAIMED IS:

1. A phase-locked loop circuit, comprising:

a multi-phase oscillator to generate more than one phases of an oscillator signal responsive to an input signal;

a pulse generator coupled with the multi-phase oscillator to generate a loop clock signal, which is a multiple of the oscillator signal and related to the number of phases; and

a comparison circuit coupled with the pulse generator to modify the input signal based upon a comparison of the loop clock signal with a reference clock signal.

2. The phase-locked loop circuit of claim 1, further comprising an output frequency divider coupled with the pulse generator to dynamically modify the loop clock signal to generate an output clock signal.

3. The phase-locked loop circuit of claim 2, wherein the output frequency divider comprises a output decrementer circuit with an output pulse latch to count transitions of the loop clock signal and transition a voltage latched to an output of the pulse latch between a high voltage and a low voltage to generate the output clock signal.

4. The phase-locked loop circuit of claim 1, wherein the multi-phase oscillator comprises a voltage controlled, ring oscillator circuit.

5. The phase-locked loop circuit of claim 1, wherein the pulse generator comprises OR gate logic to combine pulses generated in response to a transition of a phase of the more than one phases of the oscillator signal.

6. The phase-locked loop circuit of claim 5, wherein the transition of the phase comprises a rising edge.

7. The phase-locked loop circuit of claim 1, wherein the pulse generator comprises OR gate logic to combine pulses generated for each phase.

8. The phase-locked loop circuit of claim 1, wherein the comparison circuit comprises a frequency divider coupled with the pulse generator to generate a feedback control signal having a frequency comparable to a frequency associated with the reference clock signal.

9. The phase-locked loop circuit of claim 8, wherein the frequency divider comprises a feedback decrementer circuit with a feedback pulse latch to count transitions of the loop clock signal and toggle an output based upon a count of the transitions, wherein toggling the output generates the feedback signal.

10. A frequency divider, comprising:

a latch to receive a divisor having at least one bit;

a decrementer circuit to count a number of transitions of a clock signal and to output a pulse when the number reaches the divisor; and

a pulse latch circuit to transition an output voltage in response to receipt of the pulse, to generate an output clock signal having a frequency of the clock signal divided by the divisor.

11. The frequency divider of claim 10, wherein the divisor comprises two bits to divide the frequency of the clock signal by four.

12. The frequency divider of claim 10, wherein the clock signal comprises a loop clock signal generated by a pulse generator based upon a combination of multiple phases of an oscillator signal from a voltage-controlled oscillator, the loop clock signal being a multiple of the oscillator signal and related to the number of phases.

13. The frequency divider of claim 10, wherein the decrementer circuit comprises a multiplexer to decrement a divisor count from the divisor to zero and, upon reaching zero, to reload the divisor count via the latch.

14. The frequency divider of claim 13, wherein the decrementer circuit comprises a Z generator to determine when the divisor count reaches zero to transmit a pulse to the pulse latch circuit.

15. The frequency divider of claim 10, wherein the decrementer circuit comprises dynamic logic to the number of transitions of the clock signal.

16. The frequency divider of claim 10, wherein the pulse latch circuit comprises an inverter to invert the output voltage, a first latch to latch the inverted output voltage in response to a pulse from the decrementer circuit, and a second latch to latch the voltage latched at the first latch in response to a transition of the clock signal.

17. A method for generating an output clock signal based upon a reference clock signal, the method comprising:

generating phases of an oscillator signal in response to an input voltage, wherein the input voltage results from a comparison of the output clock signal and a reference clock signal;

generating pulses in response to transitions associated with the phases of the oscillator signal; and

combining the pulses to generate the output clock signal, the output clock signal being a multiple of the oscillator signal and related to the number of phases of the oscillator signal.

18. The method of claim 17, wherein further comprising dynamically adjusting a frequency of the output clock signal.

19. The method of claim 17, wherein generating phases comprises dividing the output clock signal to generate a feedback signal having a frequency comparable to a frequency of the reference clock signal to determine the input voltage.

20. The method of claim 17, wherein generating pulses comprises generating a pulse based upon rising edges of the phases of the oscillator signal.